

## Claims

[c1] 1. An integrated circuit structure comprising:  
a substrate having at least two types of crystalline orientations;  
first-type transistors formed on first portions of said substrate having a first type of crystalline orientation;  
and  
second-type transistors formed on second portions of said substrate having a second type of crystalline orientation,  
wherein selected ones of said first portions of said substrate comprise non-floating substrate portions, and  
wherein remaining ones of said first portions and all of said second portions of said substrate comprise floating substrate portions.

[c2] [c]  
2. The structure in claim 1, wherein said floating structures comprise silicon over insulator (SOI) structures.

[c3] [c]  
3. The structure in claim 1, wherein said non-floating substrate portions are biased by layers below said substrate.

[c4] [c] 4.The structure in claim 1, further comprising a complete insulator below said floating substrate portions.

[c5] [c] 5.The structure in claim 1, further comprising an incomplete insulator below said non-floating substrate portions.

[c6] [c] 6.The structure in claim 1, further comprising shallow trench isolation (STI) regions between said non-floating substrate portions and said floating substrate portions.

[c7] [c] 7.The structure in claim 1, wherein each of said second portions of said substrate includes a plurality of floating substrate portions.

[c8] [c] 8.An integrated circuit structure comprising:  
a substrate having at least two types of crystalline orientations;  
N-type transistors formed on first portions of said substrate having a first type of crystalline orientation; and  
P-type transistors formed on second portions of said substrate having a second type of crystalline orientation,

wherein selected ones of said first portions of said substrate comprise non-floating substrate portions, and wherein remaining ones of said first portions and all of said second portions of said substrate comprise floating substrate portions.

[c9] [c]

9. The structure in claim 8, wherein said floating structures comprise silicon over insulator (SOI) structures.

[c10] [c]

10. The structure in claim 8, wherein said non-floating substrate portions are biased by layers below said substrate.

[c11] [c]

11. The structure in claim 8, further comprising a complete insulator below said floating substrate portions.

[c12] [c]

12. The structure in claim 8, further comprising an incomplete insulator below said non-floating substrate portions.

[c13] [c]

13. The structure in claim 8, further comprising shallow trench isolation (STI) regions between said non-floating substrate portions and said floating substrate portions.

[c14] [c]

14. The structure in claim 8, wherein each of said second portions of said substrate includes a plurality of floating substrate portions.

[c15] [c]

15. A method of forming an integrated circuit structure, said method comprising:

forming an insulator on a first substrate structure; bonding a second substrate structure to said insulator to form a laminated structure having a first substrate with a first crystalline orientation below said insulator, and a second substrate with a second crystalline orientation above said insulator;

forming first openings in said second substrate down to said insulator;

forming second openings in said insulator through said first openings to expose said first substrate, wherein said second openings are smaller than said first openings;

growing additional material on said first substrate through said second openings to fill said first openings to produce a surface at the top of said laminated structure that has first portions having said first type of crystalline orientation and second portions having said second type of crystalline orientation;

forming first-type transistors above said first portions of said surface; and

forming second-type transistors above said second portions of said surface,

wherein ones of said first portions of said surface that are formed above said second openings in said insulator comprise non-floating substrate portions, and

wherein remaining ones of said first portions and all of said second portions of said surface comprise floating substrate portions.

[c16] [c]

16. The method in claim 15, wherein said additional material has the same crystalline orientation as said first substrate.

[c17] [c]

17. The method in claim 15, further comprising, before said forming of said first openings, forming a protective cap over said second substrate, wherein said first openings are formed through said protective cap and through said second substrate.

[c18] [c]

18. The method in claim 15, further comprising, after forming said first openings, forming an isolation material along sidewalls of said second substrate exposed by

said first openings.

[c19] [c]

19. The method in claim 15, further comprising, after said process of growing said additional material, forming shallow trench isolation (STI) structures in said first portions and said second portions to subdivide said first portions and said second portions.

[c20] [c]

20. The method in claim 20, wherein said second openings are smaller than the distance between said shallow trench isolation structures such that each of said second openings is between two adjacent shallow trench isolation structures.

[c21] [c]

21. An integrated circuit structure comprising:  
a substrate comprising a material having one type of crystalline orientation, wherein said substrate includes first portions and second portions, wherein the crystalline structure of said first portions is rotated with respect to the crystalline structure of said second portions;  
first-type fin-type field effect transistors (FinFETs) formed on said first portions of said substrate; and  
second-type FinFETs formed on said second portions of said substrate,

wherein said first-type FinFETs have fins that are parallel to fins of said second-type FinFETs.

[c22] [c]

22. The structure in claim 21, wherein said substrate comprises a floating substrate.

[c23] [c]

23. The structure in claim 22, wherein said first-type FinFETs and said second-type FinFETs comprise silicon over insulator (SOI) structures.

[c24] [c]

24. The structure in claim 22, further comprising a complete insulator below said floating substrate.

[c25] [c]

25. The structure in claim 22, further comprising shallow trench isolation (STI) regions between said first portions of said substrate and said second portions of said substrate.

[c26] [c]

26. A method of forming an integrated circuit structure, said method comprising:  
forming an insulator on a first substrate structure;  
bonding a second substrate structure to said insulator to form a laminated structure having said insulator between

said first substrate structure and said second substrate structure, wherein said first substrate structure and said second substrate structure have the same type of crystalline orientation, and wherein the crystalline structure of said first substrate structure is rotated with respect to the crystalline structure of said second substrate structure;

forming openings in said first substrate structure down to said second substrate structure; growing material on said second substrate structure through said openings to fill said openings to produce a surface at the top of said laminated structure that has first portions and second portions, wherein the crystalline structure of said first portions is rotated with respect to the crystalline structure of said second portions; forming first-type fin-type field effect transistors (FinFETs) above said first portions of said surface; and forming second-type FinFETs above said second portions of said surface.

[c27] [c]

27. The method in claim 26, further comprising, after forming said openings, forming an isolation material along sidewalls of said openings.

[c28] [c]

28. The method in claim 26, further comprising, after

said process of growing said additional material, forming shallow trench isolation (STI) structures in said first portions and said second portions to subdivide said first portions and said second portions.

[c29] [c]

29. A method of forming an integrated circuit structure, said method comprising:

forming an insulator on a first substrate structure;

bonding a second substrate structure to said insulator to form a laminated structure having said insulator between said first substrate structure and said second substrate structure, wherein said first substrate structure and said second substrate structure have the same type of crystalline orientation, and wherein the crystalline structure of said first substrate structure is rotated with respect to the crystalline structure of said second substrate structure;

forming first openings in said second substrate structure down to said insulator;

forming second openings in said insulator through said first openings to expose said first substrate structure, wherein said second openings are smaller than said first openings;

growing material on said first substrate structure through said second openings to fill said first openings

to produce a surface at the top of said laminated structure that has first portions and second portions, wherein the crystalline structure of said first portions is rotated with respect to the crystalline structure of said second portions;

forming first-type fin-type field effect transistors (FinFETs) above said first portions of said surface; and forming second-type FinFETs above said second portions of said surface,

wherein ones of said first portions of said surface that are formed above said second openings in said insulator comprise non-floating substrate portions, and wherein remaining ones of said first portions and all of said second portions of said surface comprise floating substrate portions.

[c30] [c]

30. The method in claim 29, further comprising, before said forming of said first openings, forming a protective cap over said second substrate structure, wherein said first openings are formed through said protective cap and through said second substrate.

[c31] [c]

31. The method in claim 29, further comprising, after forming said first openings, forming an isolation material along sidewalls of said second substrate exposed by

said first openings.

[c32] [c]

32.The method in claim 29, further comprising, after said process of growing said material, forming shallow trench isolation (STI) structures in said first portions and said second portions to subdivide said first portions and said second portions.

[c33] [c]

33.The method in claim 29, wherein said first substrate is rotated  $45^0$  with respect to said second substrate.

[c34] [c]

34.A method of forming an integrated circuit structure, said method comprising:  
forming an insulator on a first substrate structure with a first crystalline orientation;  
bonding a second substrate structure having a second crystalline orientation to said insulator to form a laminated structure;  
forming openings in said first substrate structure and said insulator to expose portions of said second substrate structure;  
forming a silicon germanium layer on exposed portions of said second substrate structure;  
growing material on said silicon germanium layer

through said openings to fill said openings to produce a surface at the top of said laminated structure that has first portions having said first crystalline orientation and second portions having said second crystalline orientation;

patterning said first portions and said second portions into first-type fins and second-type fins, wherein said first-type fins have said first crystalline orientation and are insulated from said second substrate by said insulator, and wherein said second-type fins have said second crystalline orientation and are positioned over said silicon germanium layer; and

changing said silicon germanium layer to an insulator layer.

- [c35] 35. The method in claim 34, further comprising, before forming said silicon germanium layer, protecting exposed sidewalls portion of said first substrate within said openings using an additional insulator.
- [c36] 36. The method in claim 34, wherein said process of changing said silicon germanium layer to an insulator layer comprises oxidizing entire thickness of said silicon germanium layer.
- [c37] 37. The method in claim 34, wherein said process of changing said silicon germanium layer to an insulator

layer comprises:

selectively removing said silicon germanium with respect to said first-type fins and said second-type fins; and forming said insulator layer on said second substrate structure.

[c38] 38. The method in claim 34, wherein said first substrate structure and said second substrate structure have the same type of crystalline orientation, and wherein the crystalline structure of said first substrate structure is rotated with respect to the crystalline structure of said second substrate structure.

[c39] [c]

39. The method in claim 34, wherein said first substrate structure and said second substrate structure have different types of crystalline orientations.